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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/605,408	09/29/2003	Kern Rim	YOR920000707US2	2407
27127	7590	02/09/2005	EXAMINER	
HARTMAN & HARTMAN, P.C. 552 EAST 700 NORTH VALPARAISO, IN 46383			MITCHELL, JAMES M	
			ART UNIT	PAPER NUMBER
			2813	

DATE MAILED: 02/09/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

H.A

<b>Office Action Summary</b>	<b>Application No.</b> 10/605,408	<b>Applicant(s)</b> KERN RIM	
	<b>Examiner</b> James M. Mitchell	<b>Art Unit</b> 2813	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

### Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

### Status

- 1) ☒ Responsive to communication(s) filed on 29 September 2003.
- 2a) ☐ This action is **FINAL**.                      2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

### Disposition of Claims

- 4) ☒ Claim(s) 1-23 is/are pending in the application.
- 4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.
- 5) ☐ Claim(s) \_\_\_\_\_ is/are allowed.
- 6) ☒ Claim(s) 1-23 is/are rejected.
- 7) ☐ Claim(s) \_\_\_\_\_ is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

### Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on \_\_\_\_\_ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.  
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

### Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All    b) ☐ Some \*    c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
  2. ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
  3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

\* See the attached detailed Office action for a list of the certified copies not received.

### Attachment(s)

- |                                                                                                                                              |                                                                                         |
|----------------------------------------------------------------------------------------------------------------------------------------------|-----------------------------------------------------------------------------------------|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892)                                                                  | 4) <input type="checkbox"/> Interview Summary (PTO-413)<br>Paper No(s)/Mail Date. _____ |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948)                                                         | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152)             |
| 3) <input checked="" type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)<br>Paper No(s)/Mail Date <u>9/29/03</u> . | 6) <input type="checkbox"/> Other: _____                                                |

### DETAILED ACTION

This office action is in response to the application filed September 29, 2003.

#### ***Claim Rejections - 35 USC § 102***

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

Claims 1-17 are rejected under 35 U.S.C. 102(e) as being anticipated by Yeo et al. (U.S. 2005/0003599).

Yeo (Fig 3, 4, 6) discloses (cl. 1, 13) a method of forming a strained silicon-on-insulator structure, the method comprising the steps of: forming a silicon layer (3) on a strain-inducing layer (2) so as to form a multilayer structure, the strain-inducing layer having a different lattice constant than silicon (Par. 0013) so that the silicon layer is strained as a result of a lattice mismatch with the strain-inducing layer, [also 5, 6, 8, 14, 15, 16] bonding <sup>1</sup> the multilayer structure to a substrate (4) so that an insulating layer (5) is between the strained silicon layer (3) and the substrate (4) [also 6] with the insulating layer comprising a first portion/ layer/ surface, top, on the substrate and a second layer, bottom, on the strained silicon layer directly contacting the insulating layer, and then removing the strain-inducing layer (500; Abstract) to expose a surface of

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the strained silicon layer (3) and to yield a strained silicon-on-insulator structure comprising the substrate (4), the insulating layer (5) on the substrate and the strained silicon layer (3) on the insulating layer; (cl. 2, 9) wherein the substrate is formed of a semiconductor material (Par 0016); (cl. 3, 4) and the inducing layer being SiGe and formed by exptaxial growth (Par. 0013); (Cl. 10, 18) and the removing step comprises cleaving (Abstract); (Cl. 11) further forming an IC device (Fig 6); (cl. 12, 19) wherein the steps of forming an IC comprise the steps of forming source drain I strain material (Par. 0010, 00018) with a channel between (i.e. "MOSFET"); (cl. 17) and bonding a first semiconductor substrate (1) to a second semiconductor (4) of the multi layer; (cl. 20, 21) with a gate (7) separated from channel by the insulating material (5) and oxide (Par. 00148).

Claims 1, 6 and 13-16 are rejected under 35 U.S.C. 102(e) as being anticipated by Cohen et al. (U.S. 2004/014254).

Cohen (Fig 6, 7) discloses (cl. 1, 13) a method of forming a strained silicon-on-insulator structure, the method comprising the steps of: forming a silicon layer (600) on a strain-inducing layer (520) so as to form a multilayer structure, the strain-inducing layer having a different lattice constant than silicon ("SiGe") so that the silicon layer is strained as a result of a lattice mismatch with the strain-inducing layer, [also 5, 6, 8, 14,15,16] bonding <sup>1</sup> the multilayer structure to a substrate (160) so that an insulating layer (150) is between the strained silicon layer (600) and the substrate (160) [also 6]

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<sup>1</sup> Because the claim does not claim a particular order, bonding the insulating layer to the substrate can occur at any phase (i.e. prior/ after contacting insulating layer to either a single silicon layer or combination silicon, strain inducing layer).

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with the insulating layer comprising a first portion/ layer/ surface, top, on the substrate and a second layer, bottom, on the strained silicon layer directly contacting the insulating layer, and then removing the strain-inducing layer (Fig 7) to expose a surface of the strained silicon layer (600) and to yield a strained silicon-on-insulator structure comprising the substrate (160), the insulating layer (150) on the substrate and the strained silicon layer (600) on the insulating layer;

***Claim Rejections - 35 USC § 103***

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

Claim 22 and 23 are rejected under 35 U.S.C. 103(a) as being unpatentable over Yeo et al. (U.S. 2005/0003599) as applied to claim 19 and further in combination with Yu (U.S. 6,391,695).

Yeo further disclose the inducing layer having a lattice constant from .2 to about 2 percent larger than lattice constant of silicon due to layer being SiGe (Par. 0013), but does not appear to use of a double gate.

Yu (Fig 9) discloses double gate (14, 38).

It would have been obvious to form a double gate structure on the substrate of Yeo in order to increase density and high drive current as taught by Yu (Col. 2, Lines 7-8, 50-52).

***Conclusion***

Any inquiry concerning this communication or earlier communications from the examiner should be directed to James M. Mitchell whose telephone number is (571) 272-1931. The examiner can normally be reached on M-F 8:00-4:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Carl Whitehead Jr. can be reached on (571) 272-1702. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Jmm  
February 4, 2005

Wael Fahmy  
SPE 2814